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Our Ref:	012.P53015 (Ser. No. 09/918,931)	**CC:**	

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As requested by you in our discussion earlier today, please find a draft set of amended claims based on a revision to your proposed Examiner's amendment. Please review and respond to me directly at 732 280 1390.

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Serial No. 09/918,931 DRAFT

1. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points;

a first buffering structure, coupled to a first one of said ingress/egress points and a first one of said mediums, including a first FIFO storage structure to stage a first plurality of egress packets, and packet diversion and insertion logic to enable post-switching pre-medium diversion and insertion of egress packets on the first one of said mediums; ~~and~~

a second buffering structure, coupled to a second one of said ingress/egress points and a second one of said mediums, including a second FIFO storage structure to stage a second plurality of egress packets, and packet diversion and insertion logic to enable post-switching pre-medium diversion and insertion of egress packets on the second one of said mediums; and

egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol,

writes an EOP at an offset from a SOP location of an egress packet to be dropped dropped, to effectuate a tail flush of said first FIFO storage structure.

2. (Cancelled) The apparatus of claim 1, further comprising egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an egress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure.

3. (Previously Presented) The apparatus of claim 1, further comprising egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure.

4. (Previously Presented) The apparatus of claim 3, wherein said egress packet write drop logic further sets a bad egress packet bit to denote for a downstream processor that an immediately preceding egress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

5. (Previously Presented) The apparatus of claim 1, further comprising a processor interface coupled to each of the first and the second buffering

structures, to respectively enable communication between the first and the second buffering structures and a first and second processor.

6. (Previously Presented) The apparatus of claim [[1]]5, wherein said first and second processors comprise Application Specific Integrated Circuits (ASICs).

7. (Previously Presented) The apparatus of claim 1, wherein said diversion and insertion are performed during data link/physical layer processing of egress packets.

8. (Previously Presented) The apparatus of claim 1, further comprising egress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said first plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said first FIPO storage structure.

9. (Previously Presented) The apparatus of claim [[1]]7, wherein said diversion and insertion and said data link/physical layer processing of egress packets are performed by a single Application Specific Integrated Circuit (ASIC).

10-24. (Cancelled)

25. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress;

a first buffering structure, coupled to a first one of said ingress/egress points and a first of said mediums, including a first FIFO storage structure to stage a first plurality of ingress packets, and packet diversion and insertion logic to enable post-medium extraction, pre-switching diversion and insertion of egress packets on the first one of said mediums; ~~and~~

a second buffering structure, coupled to a second one of said ingress/egress points and a second of said mediums, including a second FIFO storage structure to stage a second plurality of ingress packets, and packet diversion and insertion logic to enable post-medium extraction, pre-switching diversion and insertion of egress packets on the second one of said mediums; and

ingress packet write drop logic, which, in response to an overflow condition of said third FIFO storage structure, while operating under a first protocol,

writes an EOP at an offset from a SOP location of an ingress packet to be dropped, to effectuate a tail flush of said first FIFO storage structure.

26. (Cancelled) The apparatus of claim 25, further comprising ingress packet write drop logic, which, in response to an overflow condition of said third FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an ingress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure.

27. (Previously Presented) The apparatus of claim 25, further comprising ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

28. (Previously Presented) The apparatus of claim 27, wherein said ingress packet write drop logic further sets a bad ingress packet bit to denote for a system-side interface that an immediately preceding ingress packet was aborted,

while writing an EOP at the location being pointed to by the reloaded write pointer.

29. (Previously Presented) The apparatus of claim 25, further comprising a processor interface coupled to each of the first and the second buffering structures, to respectively enable communication between the first and the second buffering structures and a first and second processor.

30. (Previously Presented) The apparatus of claim 25, wherein said first and second processors comprise Application Specific Integrated Circuits (ASICs).

31. (Previously Presented) The apparatus of claim 25, wherein said diversion and insertion are performed during data link/physical layer processing of ingress packets.

32. (Previously Presented) The apparatus of claim 25, further comprising ingress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol,

multiplexes an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure.

33. (Previously Presented) The apparatus of claim 25, wherein said diversion and insertion and said data link/physical layer processing of ingress packets are performed by a single Application Specific Integrated Circuit (ASIC).

34-36. (Cancelled)

37. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch packets received through mediums coupled to the ingress/egress points; and

a buffering structure including a first FIFO storage structure, coupled to a first of said ingress/egress points and a first of said mediums, to stage a first plurality of ingress packets, and packet diversion and insertion logic to enable post-medium extraction, pre-switching diversion and insertion of egress packets on the first one of said mediums, and to enable post-switching pre-medium diversion and insertion of egress packets on the first one of said mediums; and

egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol,

writes an EOP at an offset from a SOP location of an egress packet to be dropped, to effectuate a tail flush of said first FIFO storage structure.

38. (Previously Presented) The apparatus of claim 37, further comprising a processor interface coupled to each of the first and the second buffering

structures, to respectively enable communication between the first and the second buffering structures and a first and second processor.

39. (Previously Presented) The apparatus of claim 37, wherein said diversion and insertion are performed during data link/physical layer processing of egress packets.

40. (Previously Presented) The apparatus of claim 39, wherein said diversion and insertion and said data link/physical layer processing of egress packets are performed by a single Application Specific Integrated Circuit (ASIC).

41. (Previously Presented) The apparatus of claim 37, wherein said diversion and insertion are performed during data link/physical layer processing of ingress packets.

42. (Previously Presented) The apparatus of claim 37, wherein said diversion and insertion and said data link/physical layer processing of ingress packets are performed by a single Application Specific Integrated Circuit (ASIC).

43-89. (Cancelled)